A NOVEL METHOD TO CONTROL SPACER WIDTH

FIELD OF THE INVENTION

The present invention relates generally to semiconductor fabrication and more specifically to methods of fabricating side wall spacers.

BACKGROUND OF THE INVENTION

As semiconductor devices shrink to 0.18μm, 0.15μm and 0.13μm design rules and beyond, the side wall spacer width performance is sensitive to electric test parameters such as Isat N(P), Rser (N)P and RS N^+P^+.
This will also affect the wafer acceptance test (WAT) parameters and subsequent silicide formation.

Composite side wall spacer formation is more complex in the etching module and the spacer width is difficult to control with different pattern densities. This results in unstable Isat and/or silicide bridging issues.

U.S. Patent No. 6,268,253 B1 to Yu describes a removable spacer process.

U.S. Patent No. 5,899,722 to Huang describes a double spacer process.

U.S. Patent No. 5,879,998 to Krivokapic describes a short channel device with double spacers.

SUMMARY OF THE INVENTION

Accordingly, it is an object of one or more embodiments of the present invention to provide an improved method of controlling side wall spacer width.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure having a gate electrode portion formed thereover is provided. The gate electrode portion having a top and opposing side walls. Initial spacers are formed over the opposing side walls of the gate electrode portion. The initial spacers each having an initial width that is less than the target width. The difference between the initial width of the initial spacers and the target width is determined. A second spacer layer is formed upon the initial spacers and the structure. The second spacer layer having a thickness that is equal to the determined difference between the initial width of the initial spacers and the target width. At least the second spacer layer is etched from over the initial spacers and the structure to leave second spacer layer portions extending from the initial spacers to form the final spacers.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 5 schematically illustrate a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Unless otherwise specified, all structures, layers, steps, methods, etc. may be formed or accomplished by conventional steps or methods known in the prior art.

Initial Structure - Fig. 1

As shown in Fig. 1, a gate electrode portion 14 is formed over structure 10. An underlying gate oxide layer 12 is interposed between gate portion 14 and structure 10. A first spacer layer 16 is formed over the top and sidewalls of gate electrode portion 14 and includes an L-shaped spacer portion 18 that extends as at 17 from the gate electrode portion 14 sidewalls over the structure 10. Oxide remnants 20, preferably LPTEOS as will be used for purposes of illustration hereafter, cover the sidewall portions of first spacer layer 16 as shown in Fig. 1.

Gate electrode portion 14 has a thickness of preferably from about 1000 to 3000Å and more preferably from about 1700 to 2300Å and is preferably comprised of polysilicon (poly).

Gate oxide layer 12 has a thickness of preferably from about 125 to 175Å, more preferably from about 140 to 160Å and most preferably about 150Å

and is preferably comprised of low-pressure TEOS (LPTEOS), TEOS, PECVD or SACVD and is more preferably LPTEOS.

Structure 10 is preferably a silicon substrate and is understood to possibly include a semiconductor wafer or substrate.

First spacer layer 16 has a thickness of preferably from about 250 to 350Å, more preferably from about 280 to 320Å and most preferably about 300Å and is preferably comprised of SiN.

It is noted that an optional composite ONO (silicon oxide/silicon nitride/silicon oxide) layer may be formed underneath first spacer layer 16.

Oxide Wet Dip - Fig. 2

As shown in Fig. 2, an oxide wet dip process removes the LPTEOS remnants 20 from over the gate electrode portion 14.

Feed-Forward

The (initial) width 22 of the first spacer layer 16 extending as at 17 from the gate electrode portion 14 is determined and compared to the L-shaped target spacer 32 width 30. The difference between the target spacer 32 width 30 and the (initial) width 22 of spacer portion 18 is determined and this datum/data is fed-

forward to determine the thickness 26 of the second spacer layer 31 as shown in Fig. 3 and described below.

Preferably, the (initial) width 22 of the first spacer layer 16 is intentionally formed less than the target spacer 32 width 30. The ability to precisely control the width 30 of the target/composite spacer 32 is possible through good thickness control of the second spacer layer/second SiN spacer layer 31.

Formation of Second Spacer Layer 31 - Fig. 3

As shown in Fig. 3, using this feed-forward datum/data, a second spacer layer 31 is formed over the first spacer layer 16 and the structure 10 so that its thickness 26 that equals the difference between the target spacer 32 width 30 and the (initial) width 22 of spacer portion 18. For example, if the target spacer 32 width 30 is 900Å (third column), than for the indicated (initial) widths 22 of spacer portion 18 of the first spacer layer 16 (second column) as shown in the following table, the thickness 26 of the second spacer layer 31 would be as shown (second column):

(Initial) Spacer 18 Width 22	Second Spacer Layer 31 Thickness 26	Target Spacer 32 Width 30
650Å	250Å	900Å
700Å	200Å	900Å
750Å	150Å	900Å
800Å	100Å	900Å
850Å	50Å	900Å

The width 30 of target spacer 32 is preferably from about 100 to 800Å and more preferably from about 200 to 700Å. Within these ranges, the WAT parameters (device current (I_{sat}), R_s) show good performance.

The second spacer layer 31 is preferably comprised of the same material as is the first spacer layer 16 and is preferably SiN.

Etching of the Second Spacer Layer 31 to form the Target Spacer 32 - Fig. 4

As shown in Fig. 4, the second spacer layer 31, and the portion of the first spacer layer 16 overlying the top of the gate electrode portion 14, are etched to leave spacer portion 18' and second spacer layer portion 28 extending from spacer portion 18' which combined form final composite spacer 32 having a width 30 equal to the target width 30 as the width 24 of the second spacer layer portion 28 is equivalent to the thickness 26 of the second spacer layer 31. Spacer portion 18' and second spacer layer portion 28 are indistinguishable from each other in forming the final composite spacer 32 if both are comprised of the same material, which is preferred.

Further Processing - Fig. 5

Further processing may then proceed. For example, as shown in Fig. 5, source and drain implants 40, 42 may be formed within structure 10, outboard of composite spacer 32. By forming composite spacer 32 in accordance with the

present invention, the edge of the source and drain implants 40, 42 may be definitely defined.

Respective silicide portions may also be formed over the final spacers 32.

Advantages of the Present Invention

The advantages of one or more embodiments of the present invention include:

1. improved transistor/device electrical performance; and
2. good and stable device current (I_{sat}) performance is exhibited.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.